

PECVD PROCESS

Plasma Enhanced Chemical Vapor Deposition

Plasma Enhanced TEOS (TEOS Base)

Thickness	Tolerance	Temperature Range
400A-5KA	±5%	400°C
5K-10K	±5%	400°C
10-20KA	±5%	400°C
20-40KA	±5%	400°C

WIWNU: Wafer-within-Wafer Non-Uniformity: ±5% @ Range

Low Temperature Plasma Oxide LTO (Silane Base)

400A-5KA	±5%	380°C
5KA-10KA	±5%	380°C

WIWNU: Wafer-within-Wafer Non-Uniformity: ±5% @ Range

Oxy-Nitride

400A-3KA	±5%	400°C
3KA-5KA	±5%	400°C
5KA-10KA	±5%	400°C
10KA-20KA	±5%	400°C

WIWNU: Wafer-within-Wafer Non-Uniformity: ±5% @ Range

Wafer Size

mm	Inches
100	4
125	5
150	6
200	8

Equipment / Tool

Variable Frequency / Power

1250W @ >1300 MHz
750W @ 100 – 400 kHz

Note 1:

- Incoming Inspection of Wafers.
- Variations of deposition temperature is available upon request.
- Upon inspection of wafers, additional cleaning may be required. Customer will be notified for disposition of material to receive the following:
 - SRD, Spin Rinse Dry
 - SC1/SC2
- Additional processing and or cleaning may result in an additional charge.

Note 2:

- All film deposition measurements are made on silicon test wafers.
- All multi-stack deposition measurements are made on each individual film deposition, not on the entire stack, utilizing a silicon test wafer.
- A uniformity map will be provided for each film.
- Noel is responsible for the film deposition, uniformity and thickness.
- Noel is not responsible for results of multi-stack depositions.